VOLTAGE REGULATOR WITH BYPASS FOR

MULTI-VOLTAGE STORAGE SYSTEM

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001]   The present invention is directed to voltage regulation in multivoltage supply applications, and in particular, for peripheral devices such as memory systems.

Description of the Related Art

[0002]   Non-volatile semiconductor memory is popular for a number of uses, including cellular telephones, digital cameras, personal digital assistants, mobile computing devices, non-mobile computing devices, audio and video players and other appliances. Electrical Erasable Programmable Read Only Memory (EEPROM) and flash memory are among the most popular non-volatile semiconductor memory types.

[0003]   Typical applications include the provision of one more arrays of storage elements in a memory card system, such as a memory card, which is then inserted in a host device. Both EEPROM and flash memory utilize arrays of storage elements to store one or more bits of data per element. Each element

generally includes a floating gate that is positioned above and insulated from a channel region and a semiconductor substrate. The floating gate is positioned between source and drain regions. A control gate may be provided over and insulated from a floating gate. The threshold voltage of each memory transistor is controlled by the amount of charge that has retained on the floating gate. That is, the minimum amount of voltage that must be applied to the control gate before a transistor is turned on to permit conduction between its source entering is controlled by the level of charge on the floating gate. Many EEPROMs and flash memories have a floating gate that is used to store two ranges of charges and, therefore, the memory cell can be programmed/erased between two states. Such memory cells store one byte of data. Other EEPROMs and flash memory cells store multiple ranges of charge and, therefore, such memory cells can be programmed to store multiple states. Such memory cells store multiple bytes of data.

[0004]   Improvements in processing technology have led to smaller transistor device sizes. This in turn has led to lower power supply requirements in each successive generation of transistor technology. For example, a 0.25 micron process device operates on a voltage of approximately 2.5 volts, a 0.18 micron process uses a 1.8v (+/- 10%) supply, a 0.15 micron process will use a 1.5 (+/- 10%) volt supply, 0.13 micron technology a 1.2v (+/- 10%) supply, and so on.

[0005]   Unfortunately, not all host devices supply the requisite power required by such technology. For example, older hosts may supply 3 volts to a memory system requiring only 1.8 volts. Thus, memory devices constructed with newer technologies must allow for the possibility that the host device in which

they are used will supply a higher voltage used with legacy products. Hence power level detection and voltage regulation techniques are used to provide the correct voltage to the memory device.

[0006]   Another consideration is that most regulators impose a significant voltage drop when a substantial current is drawn from the device. A voltage regulator designed to step down a legacy voltage will experience a current drop if a lower than expected voltage is supplied at the input. For example, in a conventional voltage regulator, a 3 volt host has sufficient head room to supply high current to a 1.8 volt device, but a 1.8 volt host can not supply high current with low drop to a 1.8 volt device; the output would be too low.

SUMMARY OF THE INVENTION

[0007]   The present invention, roughly described, pertains to a system and method for supplying power to a peripheral device where the voltage supplied by a host device may be the voltage required for operation of the peripheral, or a higher voltage.

[0008]   In one aspect, the invention is a memory system including a control path to a host device supplying a voltage. The system includes a voltage regulator including an input, an output and a bypass shorting the input to the output. Additionally, a voltage detector communicating with the regulator is provided. A bypass enable signal operable responsive to a signal generated by the host device indicating that the power up of the host is complete is coupled to the bypass element.

[0009]   In a further aspect, the invention comprises a method for operating a voltage regulator in a memory system. In this aspect, the method comprises the steps of: providing a voltage regulator having an input and an output, and including a bypass shorting the input to the output; setting the bypass to off prior to power up of a host device; responsive to a power up completion signal from a host device, determining the power supplied by the host; and if the power supplied by the host is below a threshold operating voltage, enabling the bypass.

[0010]   In yet another aspect, the invention comprises a peripheral device for a host system including a voltage regulator circuit. The device may include a voltage regulator having an input and an output, and a bypass element coupled to selectively short the input to the output. A bypass control signal is provided which is coupled to the bypass element and responsive to a host system power up completed signal. The bypass control signal enables the bypass element when the voltage provided by the host is below a threshold level.

[0011]   In a still further aspect, the invention comprises a memory system. The system includes a controller, a memory array; and a voltage regulator. The regulator has a shorting element between an input and an output responsive to a bypass control signal. The bypass control signal is provided by the controller responsive to a host system power up complete signal which enables the bypass element when a host supply voltage provided by the host is below a threshold level.

[0012]   These and other objects and advantages of the present invention will appear more clearly from the following description in which the preferred embodiment of the invention has been set forth in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The invention will be described with respect to the particular embodiments thereof. Other objects, features, and advantages of the invention will become apparent with reference to the specification and drawings in which:

[0014] Figure 1 depicts a block diagram of a computer system suitable for use as a host system for the memory card of the present invention.

[0015] Figure 2 depicts a block diagram of a memory card architecture.

[0016] Figure 3 is a schematic diagram depicting an example of a conventional voltage regulator used in memory cards.

[0017] Figure 4 is a graph depicting the output voltage versus the current load for two input voltages to the voltage regulator of Figure 3.

[0018] Figure 5 is a voltage regulator of the present invention.

[0019] Figure 6 is another voltage regulator of the present invention.

[0020] Figure 7 is a flowchart depicting one method of operating the voltage regulator of the present invention.

DETAILED DESCRIPTION

[0021] The invention is suitable for use with a non-volatile memory system. The system may be utilized with any number of types of host devices such as

cellular telephones, digital cameras, personal digital assistants, mobile computing devices, non-mobile computing devices and other devices. One typical host device is a computer system. It should be recognized that the system shown in Figure 1 is exemplary and any number of devices may serve as hosts for the memory card, including digital cameras, music players, computers, and the like.

[0022]   A computer system in which the various aspects of the present invention may be incorporated is illustrated generally in Figure 1. A typical computer system architecture includes a microprocessor 110 connected to a system bus 170, along with random access, main system memory 120, and at least one or more input-output devices 130, such as a keyboard, monitor, modem, and the like. Generally, one or more non-volatile storage systems are coupled to the system bus 170 as well. Typically, such a memory is a disk drive and the data stored thereon is retrieved into the system volatile memory 120 for use in current processing, and can be easily supplemented, changed or altered.

[0023]   A storage memory system 200 is also shown as coupled to the system bus 170. System 200 is constructed of a memory controller 140, connected to the computer system bus 170, and a memory array 160, which may be comprised of EEPROM integrated circuit chips. Data and instructions are communicated from the controller 140 to the memory array 160 primarily over a data line 150. Other control and status circuits between the controller 140 and the array 160 are shown in Figure 2. The controller 140 is preferably formed primarily on a single integrated circuit chip. The memory array 160 may include a number of EEPROM integrated circuit chips.

[0024]   Figure 2 is a more detailed block diagram of an exemplary memory system. The architecture shown in Figure 2 is similar to that used for a multimedia card (MMC) system. However, it will be recognized that the invention is not limited to memory systems using the MMC architecture, but finds applicability in any application where the operating voltage required by the elements of a peripheral device is fixed, but the host device supply voltage may be the required operating voltage or a higher voltage. This includes memory systems such as PC Cards, Compact Flash cards, Secure Digital Cards as well as Smart Media and Memory Stick devices.

[0025]   In the memory system 200, various lines of the memory system buses of Figure 1 are terminated in connecting pins of a card for connection with the rest of the computer system through a connector. In the block diagram of Figure 2, a memory card 200 will be coupled to a host system 275 by a bus 240. The bus may include a number of signals which are coupled directly to memory card 200. In the multimedia card (MMC) specification, seven pins are used. In the compact flash (CF) specification, 50 pins are used. Other memory system technologies use various forms of connectors, but generally all supply an operating voltage to the peripheral memory system.

[0026]   In Figure 2, only four of the signals provided by the host are shown: the command response signal (CMD), the clock signal (CLK), and the data signal (DAT) are provided from host 275 to an interface driver 220. Also shown provided by the host 275, is the supply voltage V_{DD}. Interface driver 220 communicates with the controller 140. Controller 140 is coupled to a series of storage registers 210.

[0027]   The command signal is a bidirectional command channel used for card initialization and data transfer commands. The command signal has two operation modes: open-drain for initialization mode and push-pull for fast command transfer. Commands may be sent from the multimedia card bus master to the card and responses send from the cards to the host 275. The data signal is a bidirectional data channel. The data signal operates in a push-pull fashion. Two additional supply voltage ground signals from the host 275 to card 200 and a reserved signal make up the seven pins in an MMC card. It should be understood that any number of different storage cards 200 may be utilized in the system of the present invention.

[0028]   Registers 210 store information for controller 140. In an MMC specification, five registers are defined and include an operation conditions register (OCR) stores the V_{DD} voltage profile of the card and a driver stage register (DSR) can be used to improve best performance for extended operating conditions.

[0029]   Controller 140 communicates via a memory core interface 230 with memory array 160 to read and write data to and from the array. Any number of different types of arrays, controllers interfaces, and registers may be utilized in accordance with the present invention, and operation of memory systems of this type is well documented.

[0030]   Also shown in Figure 2 is voltage detector and regulator circuitry 250. The detector and regulator 250 of the present invention ensures that the correct voltage for operating memory card 200 is supplied to the card, irrespective of the host voltage.

[0031] Figure 3 shows a standard voltage regulator 300. Voltage regulator 300 includes a comparator 310, a PMOS transistor P1, and resistors R1 and R2. A reference voltage ensures that the supply voltage V_{DD} passing from the source of transistor P1 to the drain of transistor P1 and the output of the device (OUT) is regulated to the supply voltage required at the output. As is well known in the art, voltage regulator 300 maintains a precise voltage using precision reference voltage V_{REF} to set the output voltage (OUT). An automatic controller such as amplifier 310 is used to adjust the drive of the control element P1. Resistors R1 and R2 feed a fraction of the regulator output to the comparator's negative input. The comparator that adjusts the drive to transistor P1 so that the voltage is related to the reference voltage using well known techniques.

[0032] A problem occurs with the voltage regulator of Figure 3 if the input voltage V_{DD} is significantly less than expected. While voltage regulator 300 will operate correctly for an expected, higher voltage, for example 3 volts, relative to a target regulated voltage of 1.8v, it will fail to supply a sufficient current if the voltage input is much lower, for example 1.8 volts.

[0033] This is exemplified in Figure 4 which is a graph of the voltage output V_0 versus the load current (I_{load}) for two supply voltages V_{DD} equals 3 volts in V_{DD} equals 1.8 volts in the voltage regulator of Figure 3. As noted above, a nominal operating voltage for a 1.8 volt device is 1.65 volts, represented by the dashed line on the vertical scale of Figure 4. For a supply voltage V_{DD} of 3 volts, the output current of the voltage regulator of Figure 3 is sufficient to meet the required minimal current for operating the device and the output voltage is still above a threshold required for operating the device. If the voltage input V_{DD} changes to 1.8 volts, the performance curve drops dramatically, and the output

current drops significantly to, for example, 10 mili-amps. In this case, the supply voltage is insufficient to power the memory system.

[0034]   Figure 5 shows a first embodiment of voltage regulator suitable for use in the present invention. Elements having the same characterization as those set forth in Figure 4 are numbered in the same manner.

[0035]   As shown in Figure 5, a bypass transistor P2 has been added to the configuration of Figure 3. The elements of the regulator shown in Figure 5 other than the bypass element P2 are exemplary; it should be understood that the particular circuitry used to regulate the supply voltage relative to the output of the regulator is not critical to the invention. As will be understood from the following description, the ability to short the supply voltage at the input to the output in any regulator configuration is utilized to implement the invention.

[0036]   Voltage regulator 500 allows a variance in the input voltage to accommodate hosts delivering a supply voltage sufficient to directly power a memory system (or other peripheral) and hosts providing legacy supply voltages, higher than that required by the memory system. Also shown in Figure 5 is a smoothing capacitor C1 which, for values operating in the range of 1.8 volts, may have a value of approximately 1 micro-farad. Upon application of a BYPASS signal, under the direction of the controller 160, the bypass transistor shorts the input voltage between V_{DD} and the output. Thus, in cases where the input voltage is sufficient to operate the memory system, the bypass is enabled and the voltage is provided directly to the output. In cases where the voltage is significantly higher, the voltage regulator is allowed to operate normally to reduce the voltage supplied to the output.

[0037]   Also shown in Figure 5 is detector circuitry 550, including a low voltage detection comparator 510 and sampling logic 520 which provides an output signal which can be read by controller 140. Low voltage comparator 510 provides an output signal which is high when the V_{DD} input for the memory card is below a given threshold voltage V_{TH}. This logic in conjunction with the voltage regulator 500 of Figure 5 and 600 of Figure 6 is utilized to control voltage regulation in the present invention. The logic determines whether the voltage supplied is that of the higher voltage legacy devices, or the required supply voltage of the memory system.

[0038]   Figure 6 shows an alternative embodiment to the voltage regulator shown in Figure 5. At Figure 6, additional transistors P4, P5, and P3 are shown. The additional transistors are indicated to show an alternative for ensuring that shorting VDD and the output by coupling all three transistors in the shorting path between VDD and the output is ensured. In addition, additional resistors R3 is provided so that the voltage feedback returned to comparator 310 may be selected to have the regulator provide any of a number of suitable supply voltages at the output. By applying different feedback voltages, the voltage regulator of Figure 6 may be adapted for multiple variable voltage settings. For example, the regulator in Figure 6 shows the fractional voltage returned to comparator 310 at 1.8 volts or 1.2 volts. Obvious variations of the configuration of the regulator of Figures 5 and 6 to allow for step-down of various input voltages will be readily apparent to one of average skill in the art.

[0039]   Figure 7 shows a method for operating the voltage regulator of Figures 5 or 6 in accordance with the invention. In general, the method assumes

that the supply voltage will be high and allows the host to power up based on that assumption, leaving the bypass device disabled during this phase. A control signal from the host is then utilized to indicate power-up completion, and the output of the sampling logic then used to determine whether to implement the BYPASS signal.

[0040]   Assume, for example, that a memory system operable at 1.8 volts is to be used. Upon attaching to the system, the system is not aware of whether the supply voltage will be 1.8 volts or greater. At Step 710, initially, the controller sets the bypass of transistor P2 to disabled, to ensure that memory array will not be damaged for the case of higher 3 volt operation. When a host device powers up, the ramp of the host's power over time can vary widely. The ramp may be extremely steep, indicating a rapid power up, or may be more lengthy over time.

[0041]   Next, at step 720, with the bypass set to off, the controller waits for a indicator signal from the host device that power up has been completed. In one embodiment, the threshold voltage is 2.4 volts, distinguishing between 1.8 volt +/- 10% operation or 3.0 volt +/- 10% operation. In a further embodiment, where the device is an MMC card, this signal may be CMD0 or CMD1, the initial two commands sent by a host to an MMC card which are generally used to reset all cards to idle state and request and confirm operating conditions. In other technologies, any initial signal indicating the completion of power up of the host device, specifically designed for that purpose or indicating completion by its nature may be used as the indicator signal.

[0042]   Next, at Step 730, upon receipt of the power up signal from the host device, the sampling logic 520 will test the output of the low voltage comparator

510. If the output of comparator 510 is high, this indicates that a voltage below the threshold voltage V_{th} is present. If the output is low, the V_{DD} input will have exceeded the threshold voltage indicating a higher voltage.

[0043]   At Step 740, is below the threshold LV comparator voltage, then the output of the comparator will be high and the bypass will be turned on at Step 760. If the output is low, then at Step 750, the bypass will be set to off.

[0044]   When in bypass mode, most memory cards provide over voltage protection which disables any active bypass devices whenever high voltage is later supplied. This will protect the memory core in the event the user changes the supply from, for example, 1.8 volts to 3.0 volts without using the normal power down reset required in the MMC protocol.

[0045]   Normally, in many devices, the maximum internal voltage is limited so as not to pose a reliability issue with respect to the memory core. No restriction on supply ramp rates is required when using a sufficient capacitance for C1.

[0046]   In cases where the output of the low voltage comparator 510 is high, the regulator can be shut off later by firmware in the controller to save power.

[0047]   Finally, at Step 770, bypass control will be transferred to the over voltage protection normally found in the memory systems described herein.

[0048]   The foregoing detailed description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.